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(71) Applicant RCA Corporation, (USA-Delaware), 30 Rockefeller Plaza, City and State of New York 10020, United States of America.
(72) Inventor Franco Nicola Sechi
(74) Agent and/or Address for Service Richard W. Pratt, c/o RCA International Limited, Norfolk House, 31 St. James's Square, London SW1Y 4JR.

(54) **Dual-gate field-effect transistor**

(57) An FET pellet 10 is combined with a special carrier (70, Figure 7) having a source pad 76, a drain pad 74, and first and second gate pads 78, 80 and another pad 82 to create a dual-gate FET with relatively high power handling capabilities; when conventionally combined with a carrier which contains source (S), gate (G) and drain (D) electrodes the combination provides a single-gate power FET. In the dual-gate FET some of the conventionally drain electrodes (D) are connected to the source pad 76 as source electrodes S1, some of the gate electrodes are connected to the first gate pad 78 as first gate G1 and some of the gate electrodes are connected to the second gate page 80 as second gates G2. Some conventionally source electrodes (S) are connected together by a pad 82 as interconnected

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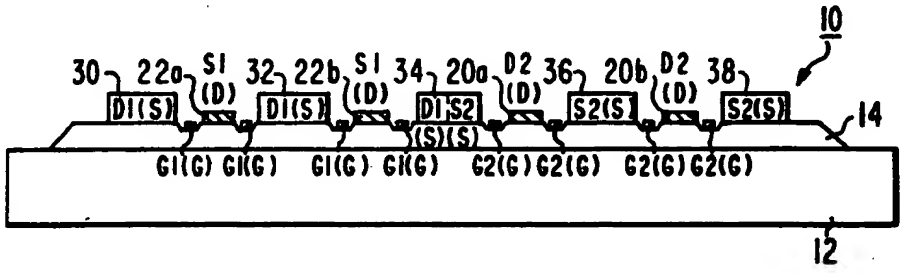

Fig. 2

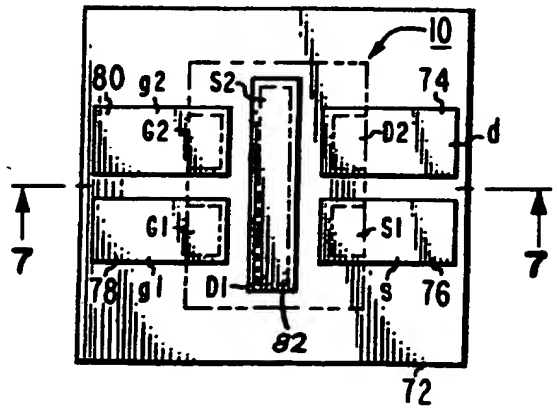

Fig. 6

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drain D1 and source S2 electrodes. Some conventionally source electrodes (S) retain the characteristics of source electrodes S2 and other conventionally source electrodes (S) have the characteristics of drain electrodes D1.

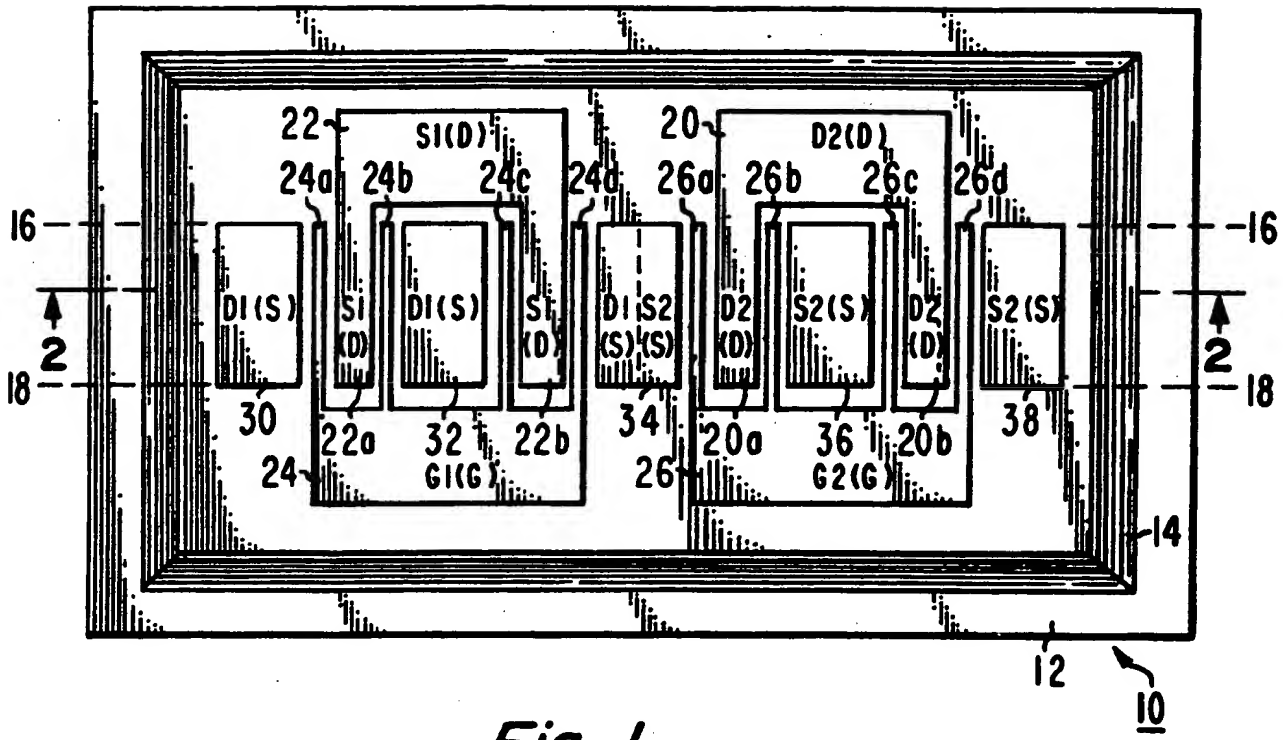
22
S1(D)
20
D2(D)
24a
24b
24c
24d
26a
26b
26c
26d
16
16
D1(S)
S1 (D)
D1(S)
S1 (D)
D1 (S)
S2 (S)
D2 (D)
S2(S)
D2 (D)
S2(S)
2
2
18
18
30
22a
32
22b
34
20a
36
20b
38
24
G1(G)
26
G2(G)
14
12
10

Fig. 1

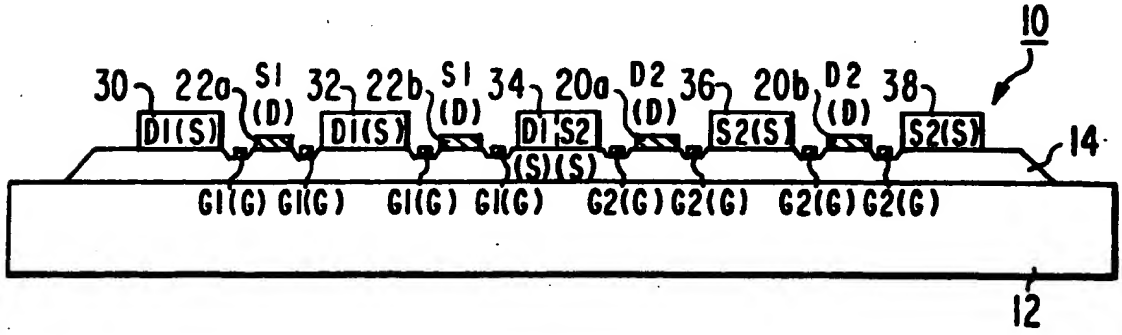
10
30
22a
S1 (D)
32
22b
S1 (D)
34
20a
D2 (D)
36
20b
D2 (D)
38
D1(S)
D1(S)
D1 S2 (S)(S)
S2(S)
S2(S)
14
G1(G) G1(G)
G1(G) G1(G)
G2(G) G2(G)
G2(G) G2(G)
12

Fig. 2

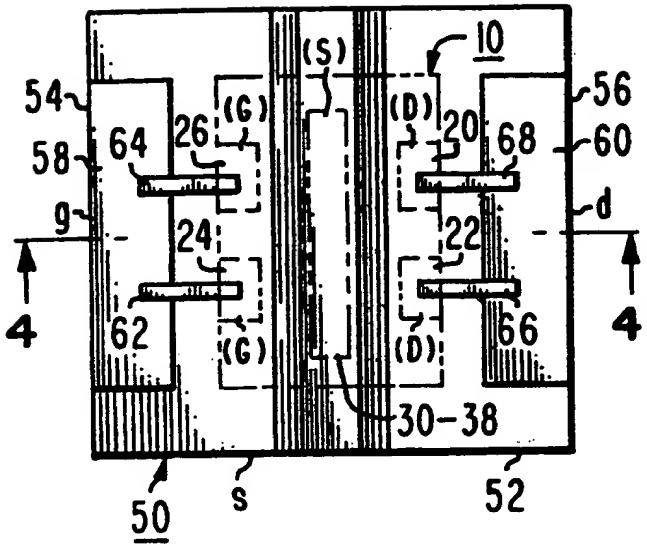

Fig. 3
PRIOR ART

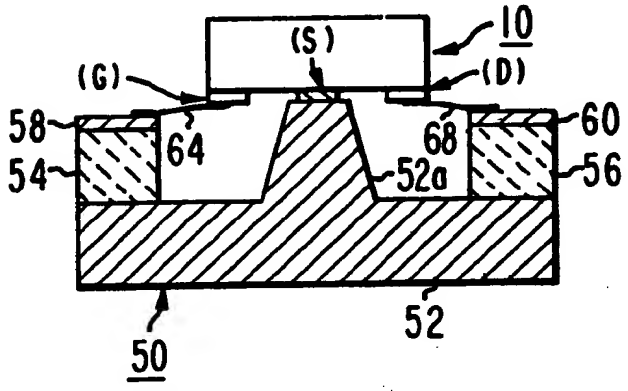

Fig. 4
PRIOR ART

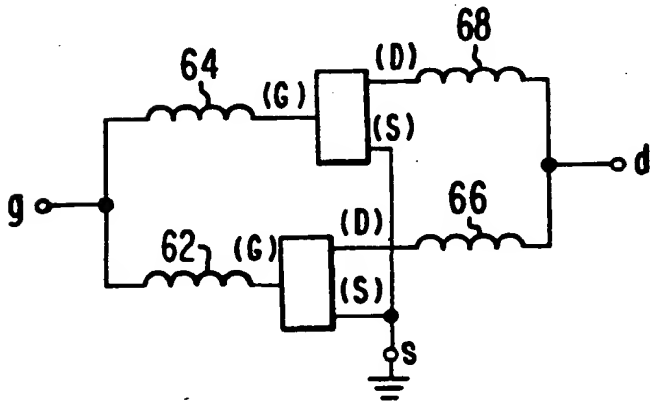

Fig. 5
PRIOR ART

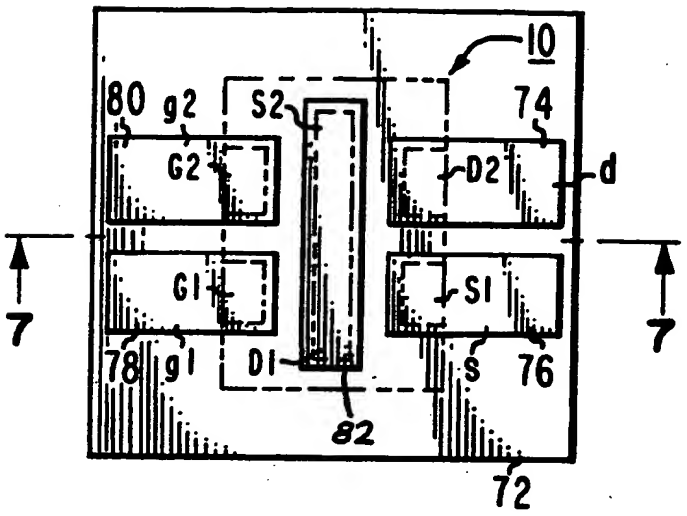

Fig. 6

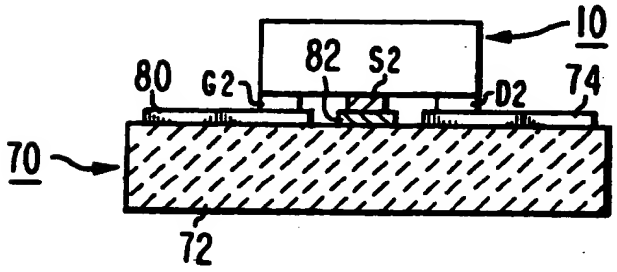

Fig. 7

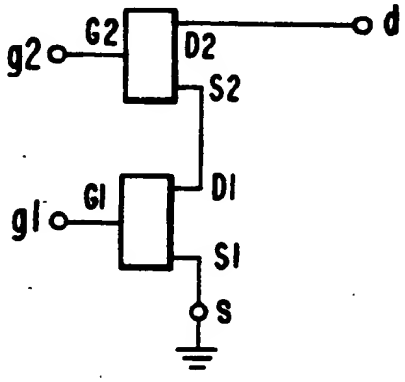

Fig. 8

SPECIFICATION

Dual-gate field-effect transistor

This invention is concerned with dual-gate field-effect transistors (FET). An illustrative application of the invention concerns dual-gate FETs which produce high power output.

Known dual-gate FETs have the desirable property of high gain at high frequencies, such as at Ku-band. Furthermore, the gain can be varied by varying the bias voltage on the second gate. Known dual-gate FETs have the undesirable property of producing low output power of approximately ten milliwatts.

Known single-gate FETs, particularly of the type described in U.S. Patent No. 3,993,515 which are "flip chip" mounted, desirably can produce hundreds of milliwatts of output power but cannot produce controlled high gain at high frequency.

In accordance with the invention; an FET pellet has at least a drain pad and a source pad and multiple electrodes connected to each of said pads, has at least two gate pads and multiple gate electrodes connected to each gate pad, and has multiple other electrodes, and a carrier comprises an electrically insulative thermally conductive substrate and, mounted thereon, a source terminal, a drain terminal, a first gate terminal, a second gate terminal, and an additional terminal. The carrier and pellet are arranged such that: the drain pad of the pellet is electrically connected to the drain terminal of the carrier, the sorce pad of the pellet is electrically connected to the source terminal of the carrier, one of said gate pads of the pellet is electrically connected to the first gate terminal of the carrier, another one of the gate pads of the pellet is electrically connected to the second gate terminal of the carrier, and the other electrodes of the pellet are electrically connected to the additional terminal of the carrier.

Figure 1 is a plan view of an FET pellet conventionally used to create a single-gate power FET;

Figure 2 is a cross section elevation view along lines 2-2 of the Figure 1 FET pellet;

Figure 3 is a plan view of a single-gate power FET carrier above which is positioned the FET pellet of Figure 1, illustrated in phantom, in accordance with the prior art;

Figure 4 is a cross section elevation view along lines 4-4 of the Figure 3 carrier and the Figure 1 pellet in accordance with the prior art;

Figure 5 is an electrical schematic of a single gate power FET constructed as in Figures 3 and 4 in accordance with the prior art;

Figure 6 is a plan view of a dual-gate power FET carrier above which is positioned the FET pellet of Figure 1, illustrated in phantom, in accordance with a preferred embodiment of the present invention;

Figure 7 is a cross section elevation view along lines 7-7 of the Figure 6 carrier and the Figure 1 pellet in accordance with a preferred embodiment of the present invention; and

Figure 8 is an electrical schematic of a dual-gate power FET constructed as in Figures 6 and 7 in accordance with a preferred embodiment of the present invention.

Referring now to Figures 1 and 2 there is illustrated, in plan view and cross sectional elevation view respectively, an FET pellet intended for use in fabricating a single-gate power FET. The pellet 10 comprises a semiconductor substrate 12 of gallium arsenide (GaAs) material upon which is deposited n-doped layer 14 approximately 0.3 micrometers thick of GaAs material. On the layer 14 is a pattern of electrodes and pads to be described hereinafter. Although the physical layout of the pads and electrodes is the same in the prior art single-gate application and the illustrative dual-gate application in accordance with the present invention, the use made of the electrodes and pads is different.

Thus in Figures 1 and 2 the letters S (source), D (drain) and G (gate) which are not in parentheses, (), refer to the use of the pads and electrodes in accordance with the invention; while the same letters enclosed in parentheses refer to the prior art use for those electrodes and pads. All electrodes, S, D and G extend between lines 16-16 and 18-18 in Figure 1. There are four pads, 20, 22, 24, and 26 illustrated in Figure 1. All electrodes and pads are typically made of gold and deposited on substrate 14.

In the prior art there are two drain pads 20, 22 by way of example. The (D) pad 20 is connected to two (D) electrodes 20a and 20b. Likewise, in the prior art there are two gate pads 24 and 26. By way of example (G) pad 26 is connected to four (G) electrodes 26a, 26b, 26c, and 26d. Referring to Figure 2, it will be noted that the upper surface of all five prior art (S) electrodes 30, 32, 34, 36 and 38 are elevated above layer 14 relative to all four (D) electrodes 20a, 20b, 22a and 22b. The eight (G) electrodes (not numbered in Figure 2 because of their small size) are depressed into voids in the layer 14 for purposes of easy manufacture. The five (S) electrodes are not connected to any source pads but rather in accordance with the prior art, are electrically connected together by a carrier to be hereinafter described. Although not indicated in Figure 2, the upper surface of pads 20, 22, 24 and 26 are at the same elevations as the upper surface of the (s) electrodes.

In a typical prior art pellet, the electrode and pad pattern illustrated in Figures 1 and 2 less one end (S) electrode (for example, 38) may be repeated. That is, a set of pads and electrodes extending between and including electrodes 30 and 26d are positioned to the left of electrode 30. Since the repeated set electrodes are not necessary to the present invention, they are not illustrated.

In accordance with the invention, the use of the various pads and electrodes is much different than the prior art use. For example, with reference to Figure 1, electrodes 22a and 22b are treated as source electrodes, not drain electrodes as in the prior art. Likewise pad 22 connected to electrodes 22a and 22b is treated as a source pad, not a drain pad. Electrodes 30, 32 and part of 34 are treated as drain electrodes, not source electrodes. Finally the gate electrodes connected to gate pad 24 are treated as gate 1 electrodes and the gate electrodes connected to gate pad 26 are treated as gate 2 electrodes

of the dual-gate FET, not simply gate electrodes of the single-gate FET.

In the prior art, FET pellet 10 is flip chip (turned over and) mounted to a carrier 50 as illustrated in plan view in Figure 3 and in cross section view in Figure 4, to which attention is now directed. Thus Figures 3 and 4 illustrate mechanically and Figure 5 illustrates electrically a single-gate power FET. With regard to Figure 3, the pellet 10 is only shown in phantom so the shape of the carrier can more easily be seen. Further, since the scale of Figures 3 and 4 are smaller than that of Figures 1 and 2, only the gate and drain pads, not electrodes are illustrated and source electrodes are simply illustrated as one long block rather than individual electrodes. Parentheses are used on the designations G, D and S to be consistent with Figures 1 and 2.

Carrier 50 includes an inverted T-shape (as viewed in Figure 4) member 52 made of copper for heat conduction and for an electrical connection to all of the source electrodes (S). For good heat dissipation characteristics the vertical portion 52a of the T is typically trapezoidal in cross section as illustrated in Figure 4. Carrier 50 also contains two ceramic risers 54 and 56 parallel to and flanking portion 52a. On each ceramic riser is a copper layer 58 and 60 respectively. Short lengths of bond wire 62 and 64 are connected between pellet gate pads 24 and 26 respectively and copper layer 58. Similarly, short lengths of bond wire 66 and 68 are connected between pellet drain pads 20 and 22 respectively and a copper layer 60. Thus, gate pads 24 and 26 are electrically connected together by copper layer 58, drain pads 20 and 22 are electrically connected together by layer 60, and the source electrodes are electrically connected together by the T-shaped area 52a which also dissipates heat produced in the source electrodes and other parts of pellet 10. Layer 58 is the transistor gate connection designated by the lower case letter g in Figure 3. Layer 56 is the transistor drain connection designated by the lower case letter d in Figure 3, and T-shaped member 52 is the transistor source connection as designated by the lower case letter s in Figure 3.

Figure 5 illustrates in electrical schematic form the transistor which is mechanically illustrated in Figures 3 and 4. The letters in parentheses () are prior art D, G and S designations corresponding with the pellet designations in Figures 1 and 2 while the lower case d, g and s terminal designations are for consistency with the equivalent designations in Figure 3.

Figures 6, 7 and 8 to which attention is directed, illustrate how the pellet of Figures 1 and 2, originally designated for use as a single-gate power FET, is used to make a dual-gate FET with power handling capacity greater than that of a conventional dual-gate FET. Figure 6 is a plan view of a dual-gate FET in accordance with the invention. The FET comprises a carrier 70 and, illustrated in phantom as was true in Figure 3, the FET pellet 10 of Figures 1 and 2. As with Figure 3, only the gate and drain (one used as a source) pads and in the general source (drain) area are illustrated. Figure 7 is a cross section elevation view along lines 7-7 of Figure 6 but with FET pellet 10 in place.

Carrier 70 comprises a substrate 72 preferably made of beryllium oxide (BeO) on which is deposited a conductive pattern typically of copper and gold. The BeO material is known to be a good electrical insulator and a good thermal conductor. The conductive pattern includes a drain pad 74 in line with and electrically connected to drain pad 20 of pellet 10, a source pad 76 in line with and electrically connected to drain pad 20 of pellet 10, a source pad 76 in line with and electrically connected to source pad 22 (a drain pad in the prior art), a first gate pad 78 in line with and electrically connected to the G1 gate pad 24 of pellet 10 and a second gate pad 80 in line with and electrically connected to the G2 gate pad 26 of pellet 10. The conductive pattern also includes a pad 82 in line with and electrically connected to all of electrodes 30, 32, 34, 36 and 38. The various pads and electrodes on pellet 10 are soldered to their associated pads on carrier 70. The heat generated in pellet 10 when it is conducting power also passes by means of the various pads to BeO substrate 72 and then to other parts of the circuit (not shown) for ultimate dissipation into the atmosphere.

The pads 74, 76, 78 and 80 are the dual-gate transistor terminals and are so indicated by lower case letters which correspond to the same letters in the dual-gate FET transistor electrical schematic of Figure 8. That is, pad 74 is the transistor drain pad d, pad 76 is the transistor source pad s, which is typically grounded as illustrated in Figure 8, pad 78 is the transistor gate g1 terminal and pad 80 is the transistor g2 gate pad terminal.

Although as illustrated in Figures 6, 7 and 8 there is no connection to the outside world from the source S2/D1 pad 82, in some applications a connection from this pad to other circuit elements (not shown) may be desirable and is easily accomplished by simply adding the desired circuitry on BeO substrate 72 interconnected as appropriate with pad 82.

By reviewing Figures 1 and 2 and Figures 6, 7 and 8 it will be understood that in accordance with the described embodiment of the invention:- some electrodes which are conventionally used as sources are instead used as drains, electrodes 30, 32 and 34 (Figure 1) being examples thereof; some electrodes which are conventionally used as drains are instead used as sources, electrodes 22a and 22b being examples thereof; the various gate electrodes which normally are electrically connected together (see Figure 3) are instead electrically split into two gates, G1 and G2; and some electrodes retain their conventional use, examples being source electrode 38 and drain electrode 20.

It will be understood that by using an FET pellet 10, Figure 1, conventionally used in making a single-gate power FET in combination with a novel carrier which interconnects the pellet electrodes differently than with the prior art carrier and provides different external connections, as illustrated in Figures 6 and 7, a dual-gate FET capable of handling power many times that of a conventional dual-gate FET is realized. Furthermore, other circuits and circuit elements

(not shown) may also be placed on the BeO substrate 72 and coupled to pads 74, 76, 78 and 80, as appropriate.

CLAIMS

1. A combination operative as a dual-gate FET; said combination comprising:

an FET pellet having at least a drain pad and a source pad, and multiple electrodes connected to each of said pads, having at least two gate pads and multiple gate electrodes connected to each of said gate pads, and having multiple other electrodes;

a carrier comprising an electrically insulative, thermally conductive substrate and mounted thereon a source terminal, drain terminal, a first gate terminal, a second gate terminal, and an additional terminal;

said carrier and pellet arranged such that said drain pad of said pellet is electrically connected to said drain terminal of said carrier, said source pad of said pellet is electrically connected to said source terminal of said carrier, one of said gate pads of said pellet is electrically connected to said first gate terminal of said carrier, another one of said gate pads of said pellet is electrically connected to said second gate terminal of said carrier, and said other electrodes of said pellet are electrically connected to said additional terminal of said carrier.

2. The dual gate FET as set forth in Claim 1 wherein said substrate is beryllium oxide.

3. The dual gate FET as set forth in Claim 2 wherein said other electrodes of said pellet serve as additional source and drain electrodes, all connected to said carrier additional terminal and not connected to any of said pellet pads.

4. The dual gate FET as set forth in any one of Claims 1, 2, and 3 wherein said electrodes are in an elongated line.

5. A dual-gate FET substantially as hereinbefore described with reference to Figures 1, 2 and 6 to 8.

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